ECE311

Design Project: Part 1

Aim: This is the first part of a bigger project where compensators will be designed to afford good stability and performance of a closed loop voltage regulator system. The power processing unit is the well-known and widely used Buck switching converter. In this first part we will simulate the open-loop performance of the converter. We will use both PECS, to perform a circuit level, large-signal simulation and Simulink to perform a transfer function level, small-signal simulation.

Tasks: The PECS schematic of the Buck regulator is shown in Figure 6.6 on page 89 of the instructor's book (which is yet to be completed, hereafter referred to as T&R (Tymerski and Rytkonen). We will however use different parameters: V_g = 100*V*, V_{out} = 40*V*, L=1 *mH*, C =100 μF, R = 10 Ω, V_M =2*V* (V_M is the peak-to-peak amplitude of the sawtooth waveform used in the Pulse Width Modulator (*PWM*), and f_s = 100*kHz* is the switching frequency. The reference voltage used is V_{ref} = *4;* this is not shown in Figure 6.6, but will be needed later. For simplicity, no losses are included in the converter.

1) Circuit level simulation using PECS

The first task is to perform a circuit level simulation using PECS. Be sure to set the correct steady state duty cycle value to produce a *40 V* output before stepping the input source. This is achieved by adjusting the level of the voltage source input to the PWM modulator.

Open loop performance will be assessed by examining the output voltage response to a 10% input voltage disturbance. The input voltage should be stepped from *100V* to *110V* and back to *100V*. This is easily performed with PECS. The response will look similar to that the response shown on page 89 for a Buck converter which uses different circuit parameters. Note that we have no interest in examining the start-up transient of the converter so please do not show this as it obscures the much smaller step input response of the converter operating in steady state.

2) Transfer function level simulation using Simulink

The step response should also be obtained using the transfer function model of the converter with Simulink. The model used is given in Figure 5.4 on page 71 of the T&R. For simplicity you can delete the Z_{out} transfer function block in the figure. The transfer functions are given in Figure 5.10 on page 78 of T&R. Use the *Ideal Case* transfer functions only. Note this a small-signal model and so the response will only show the output voltage deviations from the steady state value. The step input should be a *10 V* step, i.e. *0 V* to *10 V* back to *0 V*.

Deliverables

For both simulators show the schematics used and the responses obtained. Also show the script file used with Simulink which is run to set the parameters of the Simulink model.

Determine the following three quantities from the step response:

1) Rise time
2) Overshoot (%)
3) Settling-time (5% bounds)

Show these together in a table for both the PECS and Simulink responses. Comment on the results, i.e. how similar are they?

Provide a short description for what you are showing for all the figures.